In the Specification

Please amend paragraph [0019] on page 7 as follows:

--Figure 1 is a plan view illustrating the multiple-gate transistor of the present invention prior art;--

Please amend paragraph [0020] on page 7 as follows:

--Figure 2a is a cross-sectional view of the double-gate transistor of the present invention prior art;--

Please amend paragraph [0021] on page 7 as follows:

--Figure 2b is a cross-sectional view of the triple-gate transistor of the present invention prior art;--